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REMARKS

The application has been reviewed in light of the Office Action dated July 10, 2006. Claims 1-20 are pending. By this Amendment, claim 19 has been amended to correct an informality therein, and claims 1 and 10 have been amended to clarify the claimed invention thereof, without narrowing a scope of the claimed invention. Accordingly, claims 1-20 are presented for reconsideration, with claims 1, 10 and 19 being in independent form.

Claim 19 was objected to as having an informality.

By this Amendment, claim 19 has been amended to correct an informality therein.

Withdrawal of the objection to claim 19 is respectfully requested.

Claims 1 and 10 were rejected under 35 U.S.C. § 102(b) as purportedly anticipated by U.S. Patent No. 5,758,191 to Kasebayashi et al. Claims 2, 3, 9, 11, 12 and 18 were rejected under 35 U.S.C. § 103(a) as purportedly unpatentable over Kasebayashi in view of U.S. Patent No. 6,799,242 to Tsuda et al. Claims 4-6 and 13-15 were rejected under 35 U.S.C. § 103(a) as purportedly unpatentable over Kasebayashi and Tsuda in view of U.S. Patent No. 6,470,439 to Yamada. Claims 7, 8, 16, 17, 19 and 20 were rejected under 35 U.S.C. § 103(a) as purportedly unpatentable over Kasebayashi, Tsuda and Yamada and further in view of U.S. Patent No. 6,502,159 to Chuang.

Applicant has carefully considered the Examiner's comments and the cited art, and respectfully submits that independent claims 1, 10 and 19 are patentable over the cited art, for at least the following reasons.

This application relates to capabilities which facilitate a low power consumption mode in, for example, an optical disk drive apparatus. Applicant devised improvements which allow, for example, an optical disk drive apparatus to return from a low power consumption mode to a regular operations mode in a reliable fashion. For example, in an improved approach for communications

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interfacing, data to be transferred to a host computer is stored in a register circuit, and first information indicating a specific address of the register circuit and representing an access to a communications interface apparatus executed by the host computer for a data transfer is stored in a first memory, and second information, sent in association with the first information stored in the first memory and corresponding to the data to be transferred to the host computer, to be written into the register circuit at the specific address indicated by the first information stored in the first memory is stored in a second memory. In addition, a control circuit is provided which can perform an operation for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed. Each of independent claims 1 and 10 addresses these features, as well as additional features.

Kasebayashi (the primary reference cited in the Office Action), as understood by Applicant, proposes an approach for buffer management in a disk drive having a segment for storing burst data and another segment for write and read commands.

Kasebayashi does not teach or suggest each and every aspect of the subject matter of claim 1 of the present application.

For example, contrary to the contention in the Office Action, Kasebayashi does not disclose or suggest a second memory storing second information, sent in association with the first information stored in the first memory and corresponding to the data to be transferred to the host computer, to be written into the register circuit at the specific address indicated by the first information stored in the first memory, as provided by the subject matter of claim 1 of the present application.

The Office Action cites Figure 3 of Kasebayashi, and equates buffer 11 in Figure 3 of Kasebayashi with a register circuit storing data to be transferred to a host computer, and equates address storage unit 12 in Figure 3 of Kasebayashi with a first memory storing first information

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indicating a specific address of the register circuit.

However, it should be noted that data to be transferred to a host computer is read from the magnetic disk 13 and transferred directly to the buffer 11, and is not stored in any second memory intermediate between the magnetic disk 13 and the buffer 11.

The Office Action equates data reception unit 17 in Figure 3 of Kasebayashi with (a) a second memory storing second information, sent in association with the first information stored in the first memory and corresponding to the data to be transferred to the host computer, to be written into the register circuit at the specific address indicated by the first information stored in the first memory, and (b) a control circuit configured to perform an information writing operation for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed, in connection with the data to be transferred to the host computer.

However, while the data reception unit 17 proposed by Kasebayashi receives data sent from the host system (see Kasebayashi, column 6, lines 1-5), the data reception unit 17 does not store data to be transferred to the host computer. As is clear from Figure 3 of Kasebayashi, the data reception unit 17 does not play a role in the transfer of data to the host computer.

The Office Action also refers to data transmission unit 15 proposed by Kasebayashi. The transmission unit 15 sequentially transmits data written in the read/write area of the buffer 11 to the host system.

However, the data transmission unit 15 of Kasebayashi likewise does not disclose or suggest a second memory storing second information, sent in association with the first information stored in the first memory and corresponding to the data to be transferred to the host computer, to be written into the register circuit at the specific address indicated by the first information stored in the first

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memory.

Kasebayashi simply does not teach or suggest (a) a second memory storing second information, sent in association with the first information stored in the first memory and corresponding to the data to be transferred to the host computer, to be written into the register circuit at the specific address indicated by the first information stored in the first memory, and (b) a control circuit configured to perform an information writing operation for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed, in connection with the data to be transferred to the host computer, as provided by the subject matter of claim 1.

Tsuda, as understood by Applicant, proposes an optical disc player having a sleep mode. Fig. 7 of Tsuda shows a digital signal processor 250, a CD-ROM decoder 260, control microcomputer 244, a clock generator 62 and a buffer RAM 7 which collectively are proposed by Tsuda to be used in an optical disc player.

Tsuda, column 8, lines 11-25, proposes a process for recovering from the sleep mode to a normal operational mode. When a recovery command is received from a host computer, the recovery command is transferred from the microcomputer interface 233 of the CD-ROM decoder 260 to the control microcomputer 244, and the control microcomputer 244 in turn sends a transfer command to memory control circuit 61 of the digital signal processor 250. The memory control circuit 61 then reads TOC data stored in address register 230 of the CD-ROM decoder 260 and writes the TOC data into buffer RAM 7. The TOC data is used by the optical disc player proposed by Tsuda and is not transferred to the host computer.

Tsuda, like Kasebayashi, does not teach or suggest (a) a second memory storing second information, sent in association with the first information stored in the first memory and

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corresponding to the data to be transferred to the host computer, to be written into the register circuit at the specific address indicated by the first information stored in the first memory, and (b) a control circuit configured to perform an information writing operation for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed, in connection with the data to be transferred to the host computer, as provided by the subject matter of claim 1.

Yamada, as understood by Applicant, proposes a FIFO (first-in-first-out) memory control circuit, such as used in an electronic device, for performing asynchronous read/write control when a write clock and a read clock are different. Yamada was cited in the Office Action as purportedly proposing that the FIFO memory includes a specific number of buffer areas into which data from an external device is written.

Chuang, as understood by Applicant, proposes an approach for improving data throughput in a computer system. Chuang proposes control circuitry responsive to signals from a CPU which specify whether data from a CD-ROM is to be sent directly to a MPEG decoder circuit or to be sent to system memory.

Applicant does not find disclosure or suggestion in the cited art, however, of a communications interface including a register circuit, first and second memories and a control circuit, wherein (a) the second memory stores second information, sent in association with first information stored in the first memory and corresponding to the data to be transferred to the host computer, to be written into the register circuit at the specific address indicated by the first information stored in the first memory, and (b) the control circuit performs an information writing operation for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed, in connection with the data to be

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transferred to the host computer, as provided by the subject matter of claim 1.

Independent claim 10 is patentably distinct from the cited art for at least similar reasons.

Regarding independent claim 19 which is directed to an optical disk drive apparatus, as pointed out above, Kasebayashi relates to buffer management in the transfer of data between a hard disk and a host computer. Kasebayashi is simply not relevant to the subject matter of claim 19 of the present application.

While the Office Action lumps Kasebayashi, Tsuda and Yamada together, it would not have been obvious to one skilled in the art to apply the teachings of Kasebayashi in connection with the subject matter of claim 19 of the present application or to combine Kasebayashi with Tsuda and Yamada, since Kasebayashi is simply not relevant to an optical disk drive apparatus.

Further, as acknowledged in the Office Action, Kasebayashi, Tsuda and Yamada do not teach or suggest including, in an interface circuit for interfacing communications between a host computer and an optical disk drive mechanism of the optical disk drive apparatus, a path selection controller for controlling a buffering circuit block of the interface circuit to select the second data transfer path on an exclusive basis when the operation mode is changed from the regular operation mode to the low power consumption mode, as provided by the subject matter of claim 19 of the present application.

The Office Action equates control circuit 105 shown in Fig. 2 of Chuang to a path selection controller.

However, the control circuit 105 proposed by Chuang is part of the host computer for determining whether data received from CD-ROM drive 48 should be (a) communicated over system buses to system memory 15 or (b) routed to MPEG card 57 for decompression. The choice between (a) and (b) is made based on the type of data received from the CD-ROM drive 48, and not based on

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whether the operation mode of the CD-ROM drive is changed from the regular operation mode to the low power consumption mode.

For at least the above-stated reasons, claim 19 of the present application would not have been obvious from the cited art.

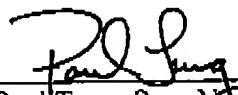
Accordingly, Applicant respectfully submits that independent claims 1, 10 and 19, and the claims depending therefrom, are patentable over the cited art.

In view of the amendments to the claims and remarks hereinabove, Applicant submits that the application is now in condition for allowance. Accordingly, Applicant earnestly solicits the allowance of the application.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Patent Office is hereby authorized to charge any fees that may be required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,


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